Claims:

What is claimed is:

1. A method for indicating reset of an integrated circuit, comprising:

setting a pin signal for a non-dedicated reset pin of an integrated circuit at a level outside of a normal range for the pin signal so that the integrated circuit is indicated to reset.

2. The method according to Claim 1, wherein setting a pin signal for a non-dedicated reset pin of an integrated circuit at a level outside of a normal range for the pin signal so that the integrated circuit is indicated to reset further comprises:

setting the pin signal below a level of the normal range for the pin signal.

3. The method according to Claim 2, wherein setting the pin signal below a level of the normal range for the pin signal further comprises:

switchingly coupling the non-dedicated reset pin directly to ground so that the pin signal is set below the level of the normal range for the pin signal and the integrated circuit is indicated to reset.

4. The method according to Claim 3, further comprising:

switchingly coupling the non-dedicated reset pin to a circuit element so that the pin signal is at a level within the normal range for the pin signal and the integrated circuit is indicated to instead operate in a normal mode.

5. The method according to Claim 4, wherein the circuit element is a capacitor coupled between the non-dedicated reset pin and ground.

6. The method according to Claim 1, wherein the non-dedicated reset pin is an analog pin.

7. The method according to Claim 6, wherein the analog pin is a quiescent voltage pin and further comprising:

coupling a voltage divider with two resistors in series between an analog power pin, that is coupled to an analog power supply, and a ground pin within the integrated circuit;

coupling the quiescent voltage pin to a node between the two resistors of the voltage divider;

switchingly coupling the quiescent voltage pin to a capacitor that is coupled to ground so that the integrated circuit is indicated to operate in a normal mode; and

switchingly coupling the quiescent voltage pin directly to ground so that the integrated circuit is indicated to reset..

8. The method according to Claim 6, wherein the analog pin is a voltage reference pin and further comprising:

coupling a resistor between an analog power pin that is coupled to an analog power supply and the voltage reference pin within the integrated circuit;

switchingly coupling the voltage reference pin to a capacitor coupled to ground so that the integrated circuit is indicated to operate in a normal mode; and

switchingly coupling the voltage reference pin directly to ground so that the integrated circuit is indicated to reset.

9. An integrated circuit, comprising:

a circuitry for an integrated circuit; and

pins coupled to the circuitry wherein one of the pins is a non-dedicated reset pin having a pin signal that is set at a level outside of a normal range for the pin signal so that the integrated circuit is indicated to reset.

10. The integrated circuit according to Claim 9, wherein the pin signal being set outside of the normal range is set below a level of the normal range for the pin signal.

11. The integrated circuit according to Claim 10, wherein the non-dedicated reset pin is switchingly coupled directly to ground so that the pin signal is set below the level of the normal range for the pin signal and the integrated circuit is indicated to reset.

12. The integrated circuit according to Claim 11, wherein the non-dedicated reset pin is switchingly coupled to a circuit element so that the pin signal is at a level within the normal range for the pin signal and the integrated circuit is indicated to instead operate in a normal mode.

13. The integrated circuit according to Claim 12, wherein the circuit element is a capacitor coupled between the non-dedicated reset pin and ground.

14. The integrated circuit according to Claim 9, wherein the non-dedicated reset pin is an analog pin.

15. The integrated circuit according to Claim 14, wherein the analog pin is a quiescent voltage pin and wherein the integrated circuit further comprises:

a voltage divider with two resistors in series coupled within the integrated circuit between an analog power pin, which is connected to an analog power supply, and a ground pin;

the quiescent voltage pin is coupled within the integrated circuit to a node between the two resistors of the voltage divider;

the quiescent voltage pin is switchingly coupled to a capacitor that is coupled to ground so that the integrated circuit is indicated to operate in a normal mode; and

the quiescent voltage pin is switchingly coupled directly to ground so that the integrated circuit is indicated to reset..

16. The integrated circuit according to Claim 14, wherein the analog pin is a voltage reference pin and wherein the integrated circuit further comprises:

a resistor coupled between an analog power pin that is coupled to an analog power supply and the voltage reference pin;

the voltage reference pin is switchingly coupled to a capacitor that is coupled to ground so that the integrated circuit is indicated to operate in a normal mode; and

the voltage reference pin is switchingly coupled directly to ground so that the integrated circuit is indicated to reset.

17. A digital-to-analog converter (DAC), comprising:

an interpolation filter for interpolating digital signals;

a delta-sigma modulator coupled to the interpolation filter wherein the delta-sigma modulator modulates the digital signals;

a digital-to-analog converter (DAC) unit with a number of DAC elements wherein the DAC unit is coupled to the delta-sigma modulator and the DAC unit converts the digital signals to analog signals;

an analog filter coupled to the DAC unit wherein the analog filter filters the analog signals; and

pins coupled to the digital-to-analog converter (DAC) wherein one of the pins is a non-dedicated reset pin having a pin signal that is set at a level outside of a normal range for the pin signal so that the DAC is indicated to reset..

18. The DAC according to Claim 17, wherein the pin signal being set outside of the normal range is set below a level of the normal range for the pin signal.

19. The DAC according to Claim 18, wherein the non-dedicated reset pin is switchingly coupled directly to ground so that the pin signal is set below the level of the normal range for the pin signal and the DAC is indicated to reset.

20. The DAC according to Claim 19, wherein the non-dedicated reset pin is switchingly coupled to a circuit element so that the pin signal is at a level within the normal range for the pin signal and the DAC is indicated to instead operate in a normal mode.

21. The DAC according to Claim 20, wherein the circuit element is a capacitor coupled between the non-dedicated reset pin and ground.

22. The DAC according to Claim 17, wherein the non-dedicated reset pin is an analog pin.

23. The DAC according to Claim 22, wherein the analog pin is a quiescent voltage pin and further comprising:

a voltage divider with two resistors in series coupled within the DAC between an analog power pin, which is connected to an analog power supply, and a ground pin;

the quiescent voltage pin is coupled to a node between the two resistors of the voltage divider;

the quiescent voltage pin is switchingly coupled to a capacitor that is coupled to ground so that the DAC is indicated to operate in a normal mode; and

the quiescent voltage pin is switchingly coupled directly to ground so that the DAC is indicated to reset..

24. The DAC according to Claim 22, wherein the analog pin is a voltage reference pin and further comprising:

a resistor coupled within the DAC between an analog power pin that is coupled to an analog power supply and the voltage reference pin;

the voltage reference pin is switchingly coupled to a capacitor that is coupled to ground so that the DAC is indicated to operate in a normal mode; and

the voltage reference pin is switchingly coupled directly to ground so that the DAC is indicated to reset.